

MCGINN & GIBB, PLLC
A PROFESSIONAL LIMITED LIABILITY COMPANY
PATENTS, TRADEMARKS, COPYRIGHTS, AND INTELLECTUAL PROPERTY LAW
8321 OLD COURTHOUSE ROAD, SUITE 200
VIENNA, VIRGINIA 22182-3817
TELEPHONE (703) 761-4100
FACSIMILE (703) 761-2375

**APPLICATION
FOR
UNITED STATES
LETTERS PATENT**

APPLICANT: Clevenger et al.

FOR: METHOD FOR PRODUCING DUAL
DAMASCENE INTERCONNECTIONS AND
STRUCTURE PRODUCED THEREBY

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METHOD FOR PRODUCING DUAL DAMASCENE INTERCONNECTIONS AND STRUCTURE PRODUCED THEREBY

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention generally relates to a method (and resultant structure) of forming a semiconductor device, and more particularly to a method (and resultant structure) of forming a dual damascene interconnection.

Description of the Related Art

10 Currently, it is difficult to adequately line contacts for copper filling at contact dimensions below 280 nm, and to line contacts reliably below contact opening sizes of less than 320 nm. This presents a major challenge to dynamic random access memory back-end-of-line (DRAM BEOL) processing that would like to migrate to a copper back-end in the near future.

15 Additionally, in the conventional methods, there are a large number of types of conducting materials that must be implemented in a BEOL process.

 Further, the conventional methods require a separate method for producing DRAM BEOL and a separate method for producing the logic BEOL so that different

manufacturing lines are required to produce either DRAM or logic with the same type and number of tools.

Finally, the conventional methods typically attempt to fill substantially both small and large structures with copper, thereby requiring additional and costly processing such as multiple CVD and advanced PVD diffusion barriers and liners which enable Cu plating.

SUMMARY OF THE INVENTION

In view of the foregoing problems, drawbacks, and disadvantages of the conventional methods, it is an object of the present invention to provide a structure and method for producing a dual damascene structure.

Another object is to fill small contacts with a highly reliable material and fill wider metal lines with, for example, copper.

In a first aspect of the present invention, a method of forming an interconnect on a semiconductor substrate, includes forming a relatively narrow first structure in a dielectric formed on a semiconductor substrate, forming a relatively wider second structure in the dielectric formed on the semiconductor substrate, forming a liner in the first and second structures such that the first structure is substantially filled and the second structure is substantially unfilled, and forming a metallization over the liner to completely fill the second structure.

In a second aspect, a method of forming an interconnect on a semiconductor substrate, includes forming a contact, including a slot, in a dielectric formed on a semiconductor substrate, forming troughs in the dielectric, thereby to form a dual damascene structure (it is noted that the order in which these levels are masked and etched may be reversed), depositing a thick conducting material on the dielectric, depositing a metal over the conducting material to completely fill the slot and metal troughs, removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric, and selectively removing the conducting material.

In a third aspect, a semiconductor device, includes a semiconductor substrate, a dual damascene structure formed in at least one dielectric film formed on the semiconductor substrate, including a relatively narrow first structure and a relatively wider second structure, a liner formed in the first and second structures such that the first structure is substantially filled and the second structure is substantially unfilled, and a metallization formed over the liner to completely fill the second structure.

With the unique and unobvious advantages of the present invention, small contacts (e.g., C1 contacts) can be filled with a highly reliable material and wider metal lines (e.g., C1 slots) with, for example, copper.

Further, the invention provides a method for easily and adequately lining contacts for copper filling at contact dimensions below 280 nm, and to lining contacts reliably below contact opening sizes of less than 320 nm.

Moreover, the invention provides a method which is advantageous from a manufacturing perspective in which the number of types of conducting materials that must be implemented in a BEOL process is minimized. Also, the same method can be used to make the DRAM BEOL and the logic BEOL. Thus, a same manufacturing line
5 can produce either DRAM or logic devices with the same type and number of tools.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a schematic diagram of a cross-section of a semiconductor chip according to the present invention;

Figure 2 is a cross-section of the chip (a wafer) after a tungsten fill;

Figure 3 is a cross-section of the semiconductor chip showing copper being
15 formed over the tungsten;

Figure 4 is a cross-section of the semiconductor chip showing a removal of the copper over the tungsten other than that in a trough (e.g., C1 slot); and

Figure 5 is a wafer cross-section after selective removal of the tungsten, either by selective etching or chemical mechanical polishing (CMP).

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to Figures 1-5, there are shown preferred embodiments of the method and structures according to the present invention.

Generally, the invention is directed to a method (and resulting structure) of forming a dual damascene interconnection.

Referring to Figure 1, in a first step of the method, contacts 101 (e.g., C1 contacts between first and second metal levels M0 and M1), including C1 slots 102 are etched into the C1/M1 dielectric 103. This dielectric can be either a nitride/oxide, low K polymer or a combination thereof.

In step 2, M1 troughs 104 are etched into the C1/M1 TEOS (or dielectric) 103. Preferably, such an etch is performed by reactive ion etching (RIE). It is noted that the order in which these levels are masked and etched may be reversed.

Thus, Figure 1 shows a cross-section of a semiconductor chip, showing the C1 contacts, C1 slots, and M1 troughs etched into the C1/M1 TEOS or dielectric to form a dual damascene structure.

Referring now to Figure 2, a thick (e.g., $<2000\text{\AA}$) reliable conducting material(s), such as a chemical vapor-deposited (CVD) metal (e.g., tungsten) is deposited on the wafer. Instead of tungsten, titanium nitride, aluminum, etc. may be used. For illustration purposes only, it will be assumed that tungsten is employed.

The thickness of the conducting material(s) is adjusted so as to substantially completely fill the relatively small C1 contacts. The small C1 contacts are typically from about 2000 to about 8000Å deep. Thus, Figure 2 shows the wafer after the tungsten fill.

Thereafter, as shown in Figure 3, a metal like copper or any other conducting material different from the first metal deposition, is then deposited over the tungsten by plating, physical vapor deposition, or chemical vapor deposition to completely fill the relatively wider lines (e.g., C1 slots and the M1 metal troughs).

Thereafter in Figure 4, the copper is polished back by CMP either to the contact fill material (e.g., tungsten) or both the copper and the contact fill material are simultaneously polished back to the dielectric.

Then, as shown in Figure 5, the tungsten is selectively removed, either by a selective etch, or by a selective CMP. Subsequent dielectric films and metal layers may be deposited on the resulting structure. Thus, Figure 5 illustrates the wafer cross-section after selective removal of the tungsten, either by selective etch or CMP.

With the unique and unobvious features of the present invention, small contacts (e.g., C1 contacts) can be filled with a highly reliable material (e.g., CVD metal) and wider metal lines (e.g., C1 slots) can be filled with, for example, copper. Thus, the invention fills the substantially smaller areas/structures with CVD metal, and the wider areas/structures are filled with copper metallization.

Further, the invention easily and adequately lines contacts for copper filling at contact dimensions below 280 nm, and lines contacts reliably below contact opening sizes of less than 320 nm.

Moreover, the invention provides a method which is advantageous from a manufacturing perspective in which the number of types of conducting materials that must be implemented in a BEOL process is minimized. Also, the same method can be used to make the DRAM BEOL and the logic BEOL. Thus, a same manufacturing line can produce either DRAM or logic devices with the same type and number of tools.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.